

ATLAS TILE Calorimeter TDAQinterface

Jul 7, 2016

University of Texas at Arlington

<http://>

Project manager

Project dates

Oct 3, 2016 - Jan 7, 2026

Completion

0%

Tasks

70

Resources

1

Tasks

2

| Name | Begin date | End date | Duration | Material | Travel |
|--|------------|----------|----------|----------|--------|
| Conceptual TDAQi demonstration <i>This first R&D phase will provide evaluation of feasibility for some critical functions using commercial solutions like FPGA evaluation boards where some of the functionalities can be emulated.</i> <i>is needed to:</i> <i>- acquire expertise on the use of components and on the programming of them.</i> <i>Also</i> <i>- acquire some of the HW that will be later used in test bench</i> | 10/3/16 | 9/29/17 | 260 | | |
| Draft of the System Requirements <i>Start outlining in an open document the requirements for the TDAQi system.</i> <i>The Interfaces with L0 and possible L1 trigger components.</i> <i>Definition of the data contents and format</i> <i>Trigger primitives: Cells, Towers, clusters.</i> <i>Latency and rates,</i> <i>Interfaces with FELIX:</i> <i>Data scheme, rates, Data format.</i> <i>Number of links required, possible speed and protocols.</i> | 10/3/16 | 11/11/16 | 30 | No | No |
| Design of test setup <i>draft of the demonstrator setup scheme. choice of the components: FPGA evaluation boards.</i> <i>Optical Link mezzanines.</i> | 11/14/16 | 12/9/16 | 20 | No | No |
| Hardware selection and procurement <i>Complete the hardware selection, contact vendors, request quotes, orde the material.</i> <i>A 30 day delay is considered as delivery time</i> | 12/12/16 | 12/30/16 | 15 | Yes | No |
| Demonstrator Setup <i>Build the Test Setup, install the needed software components</i> <i>start communication test.</i> <i>Start preparing sw tools to test basic functionality.</i> | 2/13/17 | 3/31/17 | 35 | No | No |
| PPR Link firmware <i>Implementation of the Links from the PPR PU system. TTC signal</i> <i>Characterization of Link stability, eye diagram.</i> | 4/3/17 | 5/12/17 | 30 | No | No |
| Trigger Link firmware <i>Implementation of the firmware to controll the links to the trigger components:</i> <i>Hadronic Calo,</i> <i>EM Calo,</i> <i>Muons</i> | 5/15/17 | 8/4/17 | 60 | No | No |
| Trigger primitives firmware <i>computaion of primitive for the Trigger system:</i> <i>Towers, or some other clustering for the Jet trigger.</i> <i>First layer cells for the e/gamma trigger.</i> <i>Last layer cells for the Muon trigger.</i> | 6/26/17 | 8/4/17 | 30 | No | No |

Tasks

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|--|------------|----------|----------|----------|--------|
| System Test <i>Integratipn and test of the different components:</i> <i>deserialization of input data from PPR emulator or prototype link.</i> <i>preparation of trigger primitives or passthrough data.</i> <i>Routing of data to/from FELIX emulator, TTC info.</i> <i>Routing of data to the trigger systems optical link</i> <i>Characterization of Link stability, eye diagram.</i> <i>measurement of Latency</i> | 8/7/17 | 9/29/17 | 40 | No | No |
| Qualification <i>Knowledge on components and programing is adequate.</i> <i>The latency to the trigger path is withing the specification or in reach</i> | 10/2/17 | 10/2/17 | 0 | No | No |
| TDAQi RTM Demonstrator Board <i>Design, construction and testing of the smallest scaling of the Rear Transition Module board.</i> <i>(ATCA standard)</i> <i>This will be interfaced with the PrePRocessor prototype v.1 as hosted in a comercial ATCA carrier and be able to process the data from a single Tile Module.</i> | 10/2/17 | 12/21/18 | 320 | | |
| RTM high level design <i>high level design of the RTM within the ATCA standard,</i> | 10/2/17 | 11/10/17 | 30 | No | No |
| Schematics | 11/13/17 | 2/2/18 | 60 | No | No |
| PCB Layout design | 2/5/18 | 4/27/18 | 60 | No | No |
| Component selection and procurement <i>Component selection,</i> <i>bill of material ready,</i> <i>quotes and purchasing.</i> <i>procurement time and other delay in the delivery are not included but considered as a 30 d delay before the start of the sucessor task</i> | 4/30/18 | 5/18/18 | 15 | Yes | No |
| Signal integrity Simulation <i>simulation of the layout PCB</i> | 4/30/18 | 6/22/18 | 40 | No | No |
| Internal Design Revision <i>5d: meeting at CERN or in one other hosting lab for an Informal revision of the schematics and of layout by other EE colleagues on the PPR and Tile upgrade project.</i> <i>+5 d for follow up and modifications</i> | 6/25/18 | 7/6/18 | 10 | No | Yes |
| Production of RTM Demonstrator <i>Production of PCB and testing (10d), Mounting of components (20 d) Operations done by external vendors</i> | 7/9/18 | 8/17/18 | 30 | Yes | No |
| First RTM Demo built <i>the first RTM Demonstration board have been buid</i> | 8/20/18 | 8/20/18 | 0 | No | No |

Tasks

4

| Name | Begin date | End date | Duration | Material | Travel |
|---|------------|----------|----------|----------|--------|
| Firmware revision <i>Firmware preparation for the RTM board main FPGA: tuning and optimisation of existing Fw and new Link with PPR/PU (deserialization)</i> <i>firware for local simplex IC needed for monitoring the status of the all the Optical links on the board and other basic functionality</i> | 8/7/18 | 11/26/18 | 80 | No | No |
| RTM Demonstrator testing <i>Testing of the Demonstrator board: single test of main functionality start the integration into the ATCA control</i> | 8/20/18 | 10/19/18 | 45 | Yes | No |
| Integration Test @ CERN <i>15d: preparation at UTA</i> <i>15d: at CERN, continue Integration in the ATCA system testing with the PPR PU in the ATCA carrier communication between the front and rear boards link BER and eyes diagram integration with FELIX emulator Integration with L0/L1 trigger system latency measurements</i> | 10/22/18 | 11/30/18 | 30 | Yes | Yes |
| Revision/production of second version <i>revision of the prototype and results production of a second version if needed</i> | 10/22/18 | 11/30/18 | 30 | Yes | No |
| Qualification <i>The RTM demonstrator work or mostly work some functionalities might be compromised but the issues are well understood or this is not critical for the scaling up of the board.</i> | 12/3/18 | 12/3/18 | 0 | No | No |
| Documentation <i>Updates of open document</i> | 12/3/18 | 12/21/18 | 15 | No | No |
| TDAQi Prototype <i>RTM board with the full functionality capable to read out one PPR shelf with 8 TileCal modules and route the Trigger info and data through FELIX.</i> | 12/24/18 | 3/6/20 | 315 | | |
| Schematics | 12/24/18 | 2/1/19 | 30 | No | No |
| PCB Layout design <i>Similar time (+10 d only) is assumed for the routing of the layout despite the complexity might increased a factor 4 (or 8). Considering more familiarity and similarity to the previous phase.</i> | 2/4/19 | 5/10/19 | 70 | No | No |

Tasks

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|---|------------|----------|----------|----------|--------|
| Component selection and Procurement <i>Component selection, bill of material ready, quotes and purchasing +15 days are added respect to to simialr task in the RTM Demo in case some of the components need to be replaced due resources not sufficient e/o other issues and new component need to be evaluated.</i> <i>30 d delay for procurement delivery is considered as a delay to start the successor task</i> | 5/13/19 | 6/21/19 | 30 | Yes | No |
| Signal integrity Simulation | 5/13/19 | 7/5/19 | 40 | No | No |
| Internal Design Revision <i>5d: meeting at CERN or in one other hosting lab for an Informal revision of the schematics and of layout by other EE colleagues on the PPR and Tile upgrade project. +5 d for follows up and posibles modification</i> | 7/8/19 | 7/19/19 | 10 | No | Yes |
| Production of TDAQi Prototype <i>Production of PCB and testing (10d), Mounting of components (20 d)</i> | 8/5/19 | 9/13/19 | 30 | Yes | No |
| Firmware tuning and optimisation | 9/16/19 | 11/8/19 | 40 | No | No |
| First Module Produced | 11/11/19 | 11/11/19 | 0 | | |
| Testing of the module <i>Testing of the prototype, finalization of the test setup</i> | 11/11/19 | 12/20/19 | 30 | Yes | No |
| Software <i>software for the comunication and test of the Module in the test setup</i> | 11/11/19 | 1/31/20 | 60 | No | No |
| Production of V2 Prototype <i>If needed. production of PCB and testing (10d), Mounting of components (20 d)</i> | 12/23/19 | 1/31/20 | 30 | Yes | No |
| Integration Test @ CERN <i>at CERN, Integration in the ATCA system testing with more than one PPR PU (4?) in the ATCA PPR carrier communication between the front and rear boards link BER and eyes diagram integration with FELIX or Felix emulator Integration with LO/L1 trigger system interface latency measurements</i> | 2/3/20 | 2/21/20 | 15 | No | Yes |
| Documentation <i>update of the open document and finalization of it. Specs should be frozen by now</i> | 2/24/20 | 3/6/20 | 10 | No | No |
| Integration achived | 2/24/20 | 2/24/20 | 0 | | |
| MRECF START | 4/1/20 | 4/1/20 | 0 | | |

Tasks

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|--|------------|----------|----------|----------|--------|
| TDAQi Final Design <i>This is the final iteration in the design. The system Requirements should be frozen by all meean. any possible loose end under our control are cutted. Small modification and fixes are assumed respect to the prototype.</i> | 4/6/20 | 7/31/20 | 85 | | |
| Revision of prototype <i>Revision If needed might require travel to CERN or other host Lab (5 d) plus time for preparation a/o follow up.</i> | 4/6/20 | 4/24/20 | 15 | No | Yes |
| Schematics <i>update on schematics if needed</i> | 4/27/20 | 5/15/20 | 15 | No | No |
| Component selection and Procurements <i>Revision or updates in components list and quotes and list of vendors if not satisfactory so far. Purchasing for preproduction</i> | 5/18/20 | 6/5/20 | 15 | Yes | No |
| PCB design and simulation <i>possible Revision in the layout and simulation</i> | 6/8/20 | 7/17/20 | 30 | No | No |
| Final Design Review @ CERN <i>FDR 5d travel +5 d follows up</i> | 7/20/20 | 7/31/20 | 10 | No | Yes |
| CERN FDR | 8/3/20 | 8/3/20 | 0 | | |
| TDAQi preproduction <i>TDAQi Pre-Production: 6.5.2.4.2 production of 4 RTM, finalisation of test stand for the qualification of the modules</i> | 8/3/20 | 8/20/21 | 275 | | |
| Production <i>Fabrication of PCB and Mounting of components fro 4 units</i> | 8/3/20 | 9/11/20 | 30 | Yes | No |
| Qualification <i>simple tests of the Modules</i> | 9/14/20 | 10/23/20 | 30 | No | No |
| Firmware design, testing, fixing, | 10/26/20 | 12/4/20 | 30 | No | No |
| Design of test stand <i>Test Stand for the RTM boards full testing and qualification. This is an ATCA system. Travel of EE to the Collaborating institute might be neccesary</i> | 12/7/20 | 2/26/21 | 60 | No | Yes |

Tasks

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|--|------------|----------|----------|----------|--------|
| Construction of test stand <i>Some of the equipment/components used previously only in the integration at CERN might be needed.</i> | 3/1/21 | 5/21/21 | 60 | Yes | No |
| Development of Control and Module Test <i>Development of Control and DAQ SW for the Test stand. Tuning and revision of existing components Test of the 4 units.</i> | 5/24/21 | 7/30/21 | 50 | No | No |
| Production Readiness Review <i>RPRR at CERN +Preparation</i> | 8/2/21 | 8/20/21 | 15 | No | Yes |
| CERN PRR | 8/23/21 | 8/23/21 | 0 | | |
| TDAQi production | 8/23/21 | 7/19/22 | 237 | | |
| Fabrication of PCB <i>32 units</i> | 8/23/21 | 10/1/21 | 30 | Yes | No |
| Mounting of components <i>32 units</i> | 10/4/21 | 11/12/21 | 30 | Yes | No |
| Burn in, Acceptance Testing, <i>some preliminary estimation of possible protocols for testing require ~1 week for the full validation of a board. we would like to test 2 in parallel</i> | 11/15/21 | 4/1/22 | 100 | No | No |
| Repairs of faulty units <i>repairs for 3/4 units</i> | 4/4/22 | 6/24/22 | 60 | No | No |
| Firmware finalisation | 11/15/21 | 1/21/22 | 50 | No | Yes |
| Shipment to CERN <i>shipment TBD, probably in batches of 5 units.</i> | 6/27/22 | 7/8/22 | 10 | Yes | No |
| Integration test at CERN | 7/11/22 | 7/19/22 | 7 | Yes | No |
| Acceptance at CERN | 7/20/22 | 7/20/22 | 0 | | |
| TDAQi installation | 9/2/24 | 4/25/25 | 170 | | |
| commissioning and integration test | 9/2/24 | 1/3/25 | 90 | Yes | Yes |
| software and firmware | 2/3/25 | 4/25/25 | 60 | No | No |

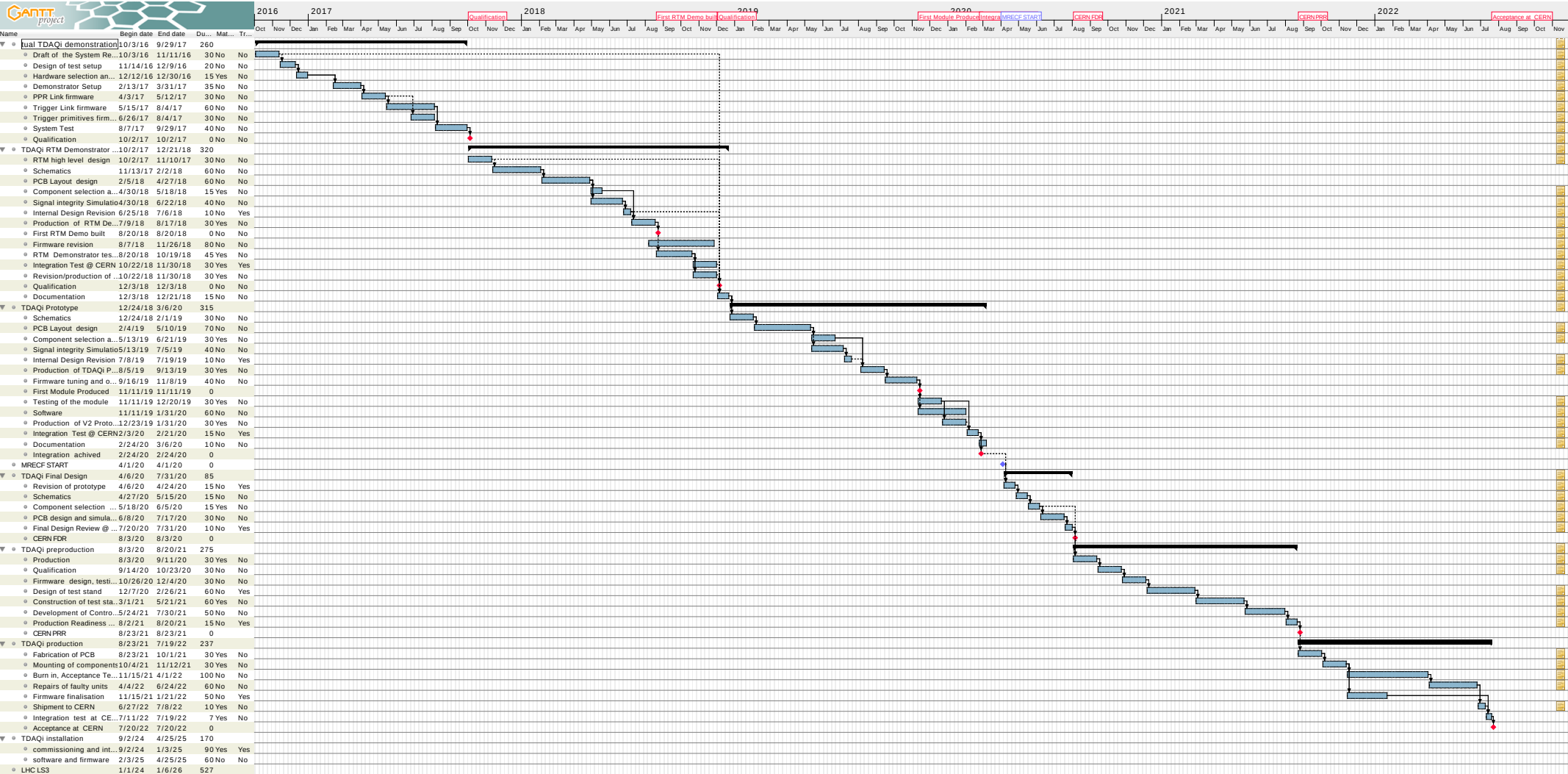
Tasks

| Name | Begin date | End date | Duration | Material | Travel |
|---------|------------|----------|----------|----------|--------|
| LHC LS3 | 1/1/24 | 1/6/26 | 527 | | |

Resources

| Name | Default role |
|------------------|--------------|
| Seyedali Moayedi | developer |

Gantt Chart



Resources Chart

